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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,737	01/14/2000	Hansjorg Reichert	GR-97-P-1903	8769

24131 7590 07/23/2004

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/483,737	REICHERT ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 15* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/9/2004 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation "using said solder to form a direct chip-substrate connection" is not disclosed in the specification to enable one skilled in the art to make and/or use the invention. Since the specification describes both the solder and the adhesive layer as being deposited on the rear side of the chip and that the solder is used to form a direct chip-substrate connection as recited in claim 15, it would take undue experimentation to make and use the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 15, as understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. ("Yamagishi") (JP 6-291239) in view of Komata et al. ("Komata") (JP 2-15897), Bacon et al. ("Bacon") USPN 5,234,153 and Lin ("Lin") USPN 4,791,075.

Yamagishi discloses in fig. 1c a solder containing at least two components with at least two constituents including a first constituent containing a precious metal and a second constituent being consumed during a soldering operation by one of reacting and being dissolved in material which are to be joined; a substrate 1; and a semiconductor chip 4 secured to said substrate by one of alloying and brazing using said solder, but do not teach a hypereutectic composition of Au-Sn with a thickness.

Komata discloses a precious metal and tin solder 13 and said solder has a hypereutectic concentration containing gold-tin (AuSn) with a hypereutectic Sn concentration and containing a gold-tin compound (AuSn) having a composition, which falls within the range recited in the claim.

Bacon teaches (see col. 1 lines 50-63 and claim 7) the advantage of using a thin gold-tin compound solder.

Lin discloses (col. 3, lines 59-67) in fig. 2 a semiconductor chip 26 having a rear side and adhesive 28 said semiconductor chip being secured to a substrate 12 using a solder 28 to form a direct chip-substrate connection.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace the Au-Sn eutectic alloy of Yamagishi with of Komata's hypereutectic Sn concentration, since that would prevent deformation thereby enhancing the mechanical strength of a semiconductor chip connection to a substrate. It would have been obvious to form a layer with a thickness of 1 μm to 2 μm, since that would provide a better thermal conductance as taught by Bacon; it would have been obvious to form a direct chip-substrate connection, since that would provide a direct heat dissipation.

6. Claim 15, as understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi in view of Ishii (JP 6-326210), Bacon and Lin.

Yamagishi discloses in fig. 1c a solder containing at least two components with at least two constituents including a first constituent containing a precious metal and a second constituent being consumed during a soldering operation by one of reacting and being dissolved in material which are to be joined; a substrate 1; and a semiconductor chip 4 secured to said substrate by one of alloying and brazing using said solder, but do not teach a hypereutectic composition of Au-Sn with a thickness.

Ishii discloses (see fig. 2 and attached machine translated version) a semiconductor chip 1 secured to a substrate 40 by gold and tin solder 8 and said solder has a hypereutectic concentration containing gold-tin (AuSn) with a hypereutectic Sn concentration and containing a

gold-tin compound (AuSn) having a composition which falls within the range recited in the claim.

Bacon teaches (see col. 1 lines 50-63 and claim 7) the advantage of using a thin gold-tin compound solder.

Lin discloses (col. 3, lines 59-67) in fig. 2 a semiconductor chip 26 having a rear side and adhesive 28 said semiconductor chip being secured to a substrate 12 using a solder 28 to form a direct chip-substrate connection.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace Yamagishi's Au-Sn eutectic alloy of with Ishii's hypereutectic Sn concentration, since that would prevent deformation thereby enhancing the mechanical strength of a semiconductor chip connection to a substrate. It would have been obvious to form a layer with a thickness of 1 μm to 2 μm, since that would provide a better thermal conductance as taught by Bacon; it would have been obvious to form a direct chip-substrate connection, since that would provide a direct heat dissipation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
July 22, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800